[0044] (2) Input stage PMOS g_m - g_m stage **101** with a differential transistor pair ~~M1-M2~~ M0-M1, diodes ~~M3-M4~~ M2-M3 and a constant tail current source **M14** is added. In this case, the gate of **M14** is tied to a constant voltage reference and the body connections of the ~~diode~~ differential transistor pair are tied to the positive supply.

[0045] (3) Squeezable current source **103**, including transistors **M15-M19**, **M57**, is added to the circuit, compared to the circuit corresponding to the graph of (2).

[0046] (4) The bodies (substrates) of the diodes ~~M3-M4~~ M2-M3 are tied to their respective sources, compared to the circuit corresponding to the graph of (3).

[0047] With each successive circuit change, the CMIR over which the gain remains relatively constant increases. This increases the range of V_{CMI} that a signal may pass with little distortion.

[0048] Thus, the present invention provides an operational amplifier with a first stage that inputs a differential input signal and absorbing common mode variations in the differential input signal, and that outputs a first differential signal. The input stage includes a differential transistor pair receiving the first differential signal from the first stage. An output stage is connected to the input stage and outputs an amplified signal corresponding to the first differential signal.

[0049] The list below shows exemplary dimensions of one embodiment of the present invention:

[0050] **M0** characteristics: w (width) = 10 μm, l (length) = 0.24 μm, m (multiplicity) = 12

M1 characteristics: w = 10 μm, l = 0.24 μm, m = 48

M2 characteristics: w = 10 μm, l = 0.24 μm, m = 12

M3 characteristics: w = 10 μm, l = 0.24 μm, m = 12

M4 characteristics: w = 10 μm, l = 0.24 μm, m = 12

M5 characteristics: w = 10 μm, l = 0.24 μm, m = 12

M8 characteristics: w = 10 μm, l = 0.4 μm, m = 32

M9 characteristics: w = 10 μm, l = 0.4 μm, m = 32

M10 characteristics: w = 10 μm, l = 0.24 μm, m = 16